

W-CSP Technology

Wafer-level Chip Size Package

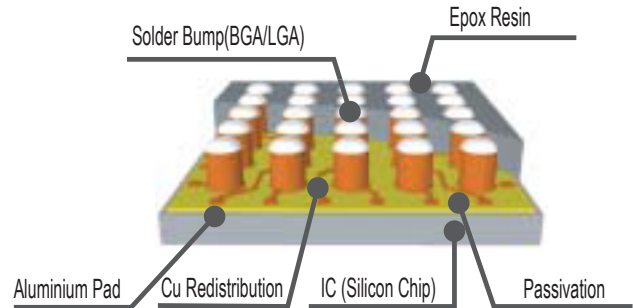
Structure of W-CSP

Structure of CASIO MICRONICS's W-CSP is shown in the illustration.

W-CSP can be differentiated from other IC packages by its unique production method that all the W-CSP packaging processes are carried out on a single silicon wafer.

Aluminum pads are interconnected by Cu redistribution wirings to Cu posts.

Epoxy resin is filled to protect the structure. Solder bumps (both eutectic and lead-free) are applied on the Cu posts.



Benefits of W-CSP

*Reduced form factor

(Small footprint: 1/4 compared to QFP, Reduced package height: less than 0.65mm/LGA, less than 0.80mm/BGA)

*Conventional SMT chip bonders can be used for mounting W-CSP's on the PCB.

*Cost benefit can be obtained if high yield and small size IC's are processed as the process cost is wafer dependent.

Reliability Data of W-CSP/Package Options

Package Option		Item	Condition	Result
Pitch	Sphere Diameter			
0.30mm	0.20mm (Ball) 0.08mm (Printing)	Moisture sensitivity HTS THB Autoclave(PCT) HAST(PCBT) Temp cycle(PKG) Temp cycle(PCB)	JEDEC level 1 @260°C(After 85°C/85%/168h) 150°C 85°C/85%/10V(L/S:10µm/10µm) 121°C/0.2026MPa(2atm) 130°C/85%/3.5V(L/S:10µm/10µm) 130°C/85%/10V(L/S:10µm/10µm) -65/+150°C -25/+125°C(7×7array/0.5mm pitch/Ball/0.1% failure)	10 times PASS 2,000 hours PASS 2,000 hours PASS 500 hours PASS 500 hours PASS 168 hours PASS 1,000 cycles PASS 900 cycles PASS
0.40mm	0.25mm (Ball) 0.08mm (Printing)			
0.50mm	0.30mm (Ball) 0.08mm (Printing)			